Parallelizing Hardware by Unfolding Algorithm for FIFOs

Degree programme: BSc in Electrical- and Communication Engineering | Specialisation: Embedded Systems
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Parallel processing is used to increase speed or reduce energy consumption in digital designs. In order to parallelize a digital design, it must be unfolded by an algorithm. The classical algorithms fail when the structure of a design is inaccessible. That is the case for intellectual property (IP) cores. In this thesis a novel algorithm that is capable of unfolding a First-In-First-Out (FIFO) IP core without accessing its structure is introduced, implemented and verified.

Motivation

A FIFO buffer is a very general and widely used data structure enabling data exchange between systems with different schedules of data processing. Since FIFO buffers are extensively used in various sorts of applications they can be regarded as standard building blocks of digital systems and therefore many different IP core FIFO buffer types can be found in custom IP core libraries.

Hardware parallelization on the other hand is a prominent method to increase the speed or to reduce the power consumption of digital designs. Classical methods of hardware parallelization may fail when IP cores are used in digital designs. IP cores are highly optimized blocks of logic and can be regarded as black boxes because the structures of such IP cores are protected against access. The availability of IP core libraries however, is a crucial aspect in digital design development since it reduces development time dramatically. Therefore new ways of parallelization must be found for designs containing IP cores.

Finding a way to enable parallel processing of IP core FIFOs would open up interesting opportunities.

Objectives

Professor Marcel Jacomet and his team at the Institute for Human Centered Engineering found a way to parallelize FIFOs without accessing the structures of the FIFOs. The FIFOs are used as whole blocks and therefore IP core FIFOs can enter the design. Two blocks of logic, the input router and the output router illustrated in the conceptual diagram, control the flow of data and control signals. The primary objective of this Bachelor Thesis is to introduce, implement and verify this novel unfolding algorithm used to parallelize IP core FIFOs.

Approach

In order to verify the correctness of the algorithm a suitable IP core FIFO is selected as a reference model and its behavior is analyzed in detail. A replicated model is developed and simulated. The structure of the replicated model is both known and accessible and can therefore be exposed to a classical procedure of parallelization. The IP core FIFO on the other hand is parallelized according to the novel algorithm. The two parallelized models using equivalent FIFO models are simulated and compared. If the simulation shows equivalence, the correctness of the algorithm is plausible.

Result

All models were implemented using hardware description language (VHDL). A VHDL testbench was used to simulate the behavior of the different models. First it was shown that the replication and the original IP core FIFO have equivalent behavior. Then the two parallelized models to be tested for equivalence were added. The behavior of the models differs only in irrelevant aspects. Therefore the novel algorithm can be regarded as correct.

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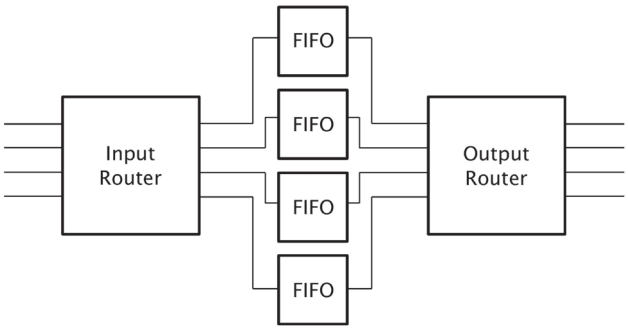

Conceptual diagram