Low-Power Hardware-based Two-stage ECG Compression for Continuous Cardiac Monitoring

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With rising cases of cardiac arrhythmias, long-term ECG monitoring is essential. While Insertable Cardiac Monitors (ICMs) offer a reliable alternative to Holter monitors, they store only short arrhythmic episodes, complicating classification. Continuous recording demands low-power ECG compression to meet volume and energy constraints. The developed algorithm achieves up to 5.7× compression with just 0.3 % PRD at below 200 nW.

Evaluation

A two-stage electrocardiogram (ECG) compression algorithm inspired by two research papers was developed, implemented in Python, and tested using the MIT-BIH Arrhythmia Database (ECGs resampled at 256 Hz, 11 bits), with added Gaussian noise. The lossy stage quantizes the input samples with **k** bits less to a low-resolution signal, which is superimposed by impulses with amplitude 1 LSB whenever the accumulated error exceeds 2^k. The resulting pulse-width-modulated (PWM) signal is stored using Huffman entropy encoding. The lossless Huffman stage must be trained on a data set such that the most frequent PWM signal values are encoded with the least number of bits.

Hardware Implementation

The algorithm was translated into VHDL and simulated using the open-source GHDL simulator. It was then synthesized with Genus, placed and routed using Innovus, and post-layout simulated in Xcelium via X-FAB's 180 nm Cadence-based ASIC flow. The post-layout results were verified against GHDL simulations. Finally, a vector-based power analysis was performed using 2 seconds of MIT-BIH ECG data as input.

Results

The algorithm achieved an average compression factor (CF) of 5.7 with Root Mean Square Difference (PRD) <0.3 % using **k** = 5 bit quantization (lossy stage CF = 11 bit/6 bit = 1.83). The CF dropped only slightly (by 0.5) under high noise (10× LSB rms). The Huffman encoding stage alone yielded just a CF of 2.44. Hardware simulations matched Python results in CF and PRD. ASIC post-layout simulations at 1.8 V showed <200 nW power consumption and <150 µm × 150 µm chip area per compression unit.

Conclusion

The two-stage ECG compression algorithm offers high compression and low complexity with minimal power overhead, thereby advancing the development of continuous ICMs.

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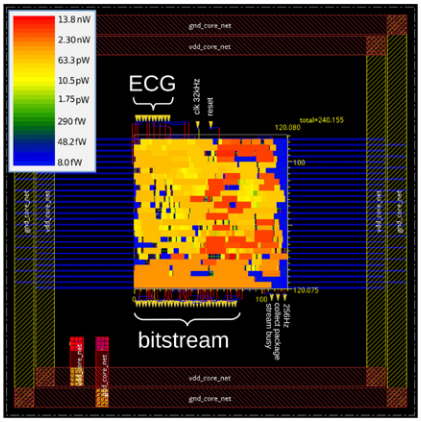

Fig. 2: Cadence power simulation (fs=256 Hz, k=5)

Fig. 1: CF and PRD vs. k and LBS rms noise