Proof of Concept: FPGA-SoC-Based Flowmeter

Degree programme: BSc in Electrical Engineering and Information Technology
Specialisation: Embedded Systems
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The FLOWave sensor from Bürkert uses contactless flow measurement based on surface acoustic waves (SAW), ensuring a hygienic and robust design. This work integrates two subsystems into a single FPGA-SoC platform for precise flow measurement. The proof of concept enables higher accuracy and faster signal processing compared to microcontroller-based systems and forms the basis for an objective performance comparison.

Background

Bürkert's FLOWave technology enables contactless flow measurement via surface acoustic waves (SAW), ensuring hygienic operation as only a stainless-steel tube contacts the medium. The current microcontroller-based system handles standard tasks but struggles with increasing demands for accuracy, sampling speed, and advanced processing, as microcontrollers lack parallelization for real-time tasks. FPGA-SoC platforms, combining programmable logic and embedded processors, provide high-speed parallel processing and hardware acceleration. This proof of concept uses a Red Pitaya board with a Xilinx Zynq-7020 FPGA-SoC and a FLOWave extension board. Previously, the signal acquisition and processing subsystems were implemented separately due to resource limits.

Goal

The aim was to integrate both subsystems into a single FPGA-SoC platform, leveraging parallelization and computational power to overcome microcontroller limitations. The FPGA-based flowmeter serves as proof of concept for benchmarking improvements in accuracy, sampling speed, and overall performance.

Implementation

The project began by analyzing anomalies and distortions in the acquisition subsystem, which were traced to internal resonances in the extension board rather than design flaws. Targeted hardware optimizations mitigated these effects. Integration required combining VHDL modules, Vivado block designs, microcontroller firmware, and control software. To fit the Zynq-7020 resource limits, FPGA utilization was reduced through trade-offs between memory and computational complexity, including optimized data paths and streamlined pipelines.

Results and Outlook

Resonance-inducing components were identified for future hardware revisions. Integration of acquisition and processing was largely successful, resolving resource, clock domain, and timing issues, and the processing subsystem was fully validated. Two AXI configuration registers in the acquisition module remain inaccessible, preventing full testing and requiring further FPGA analysis. The FPGA-SoC reduces processing time from 23.92 ms (STM32, 80 MHz) to 1.6 ms, achieving ~15× acceleration despite only ~1.5× higher clock frequency due to parallel execution.

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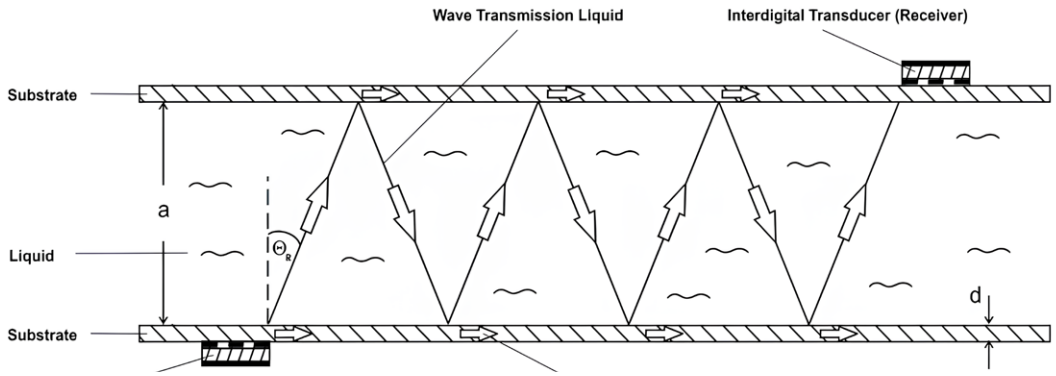

FLOWave principle: Piezo elements create acoustic waves in the fluid, with travel time depending on flow rate.